PURDUE MATERIALS ENGINEERING

Investigation of Microstructural Evolution in Advanced 3-D Logic and Memory Devices

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Three-dimensional logic and memory devices are increasing in popularity due to increases in computational power while minimizing space. However, this change in structure plays into the question of reliability of the solder joints within each layer of the device. This project seeks to explore the effects of various extended use regimes on small 3D solder joints. Intermetallic compound (IMC) growth is measured after thermal aging and the relative damage in the solder joint is assessed to provide a better qualitative and quantitative measure of the joint reliability.

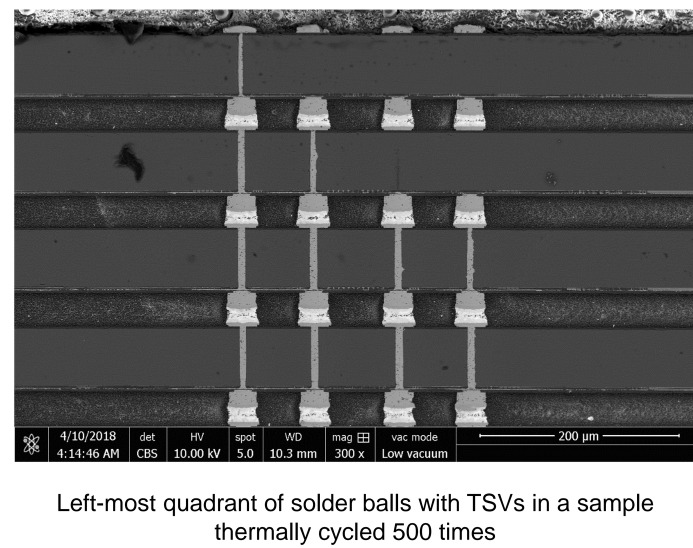
This work is sponsored by Juniper Networks, based in Sunnyvale California.

Project Motivation & Goals

By stacking layers of logic and memory devices in a 3-Dimensional architecture, systems can utilize less space and increase computation via shorter signal pathways. However, it is relatively unknown how this new architecture will affect the reliability of the solder joints, a vital component. Statistically significant data must be obtained to analyze the response of the solder to different stress states. During fabrication, the tin alloy is reflowed to attach each layer; the solder joint on the bottom level has seen 3 more heat cycles than the top level. As the 3D device thermally expands, the solder on the edges will experience a greater overall displacement and resulting in larger forces applied. Thermal aging can be utilized to assess solder damage.

Objectives:

- Measure IMC growth relative to thermal aging
- Analyze damage to solder ball
- Characterize geometric effect to reliability



Left-most quadrant of solder balls with TSVs in a sample thermally cycled 500 times

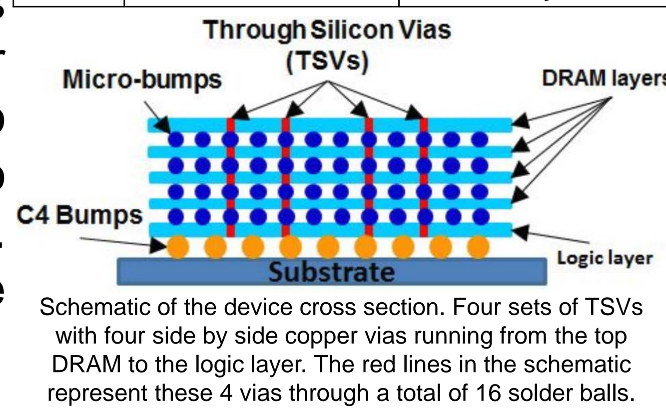
Experimental Setup & Procedure

Three tests were used to thermally age 3D memory chips: high temperature hold (HTH), thermal cycling (TC), and a sequential (SEQ) test of HTH and TC.

Thermal Testing

Test	Treatment	Read Points
HTH	150°C	500 hours 1000 hours 1500 hours
TC	-55°C - 125°C	500 cycles 1000 cycles
SEQ	150°C -55°C - 125°C	250 hour/cycles 500 hour/cycles

At each read point, the analysis focused on four sections of the chip, the four sets of Through Silicon Vias (TSVs) and the solder bumps attaching them. The four points of interest consist of 16 solder bump/TSVs each, with the outer two and inner two being equivalent due to axisymmetric geometry. At each point, the solder is analyzed for relative damage and IMC growth. Using BSE SEM imaging, the IMC layers can be determined by contrast and their thickness measured. Using the same image, the damage is measured. The damage exists as necking, large single cracks, and regions of numerous small cracks. The damage is defined as the percentage of the width that the cracks/necking extend across the solder ball, hence, 100% damage (or a score of 10/10) will have cracks extending the entire width, preventing electronic transport through the solder ball and TSV. Damage, especially cracking, will enable both electrical and mechanical failure of the device. Hence, it is vital to understand the effects of geometry and dimensionality on damage.

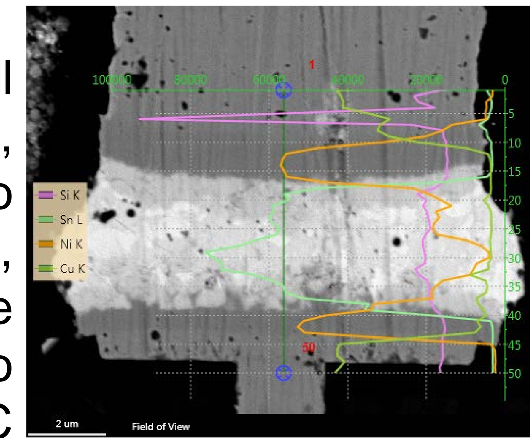


Schematic of the device cross section. Four sets of TSVs with four side by side copper vias running from the top DRAM to the logic layer. The red lines in the schematic represent these 4 vias through a total of 16 solder balls.

Results & Discussion

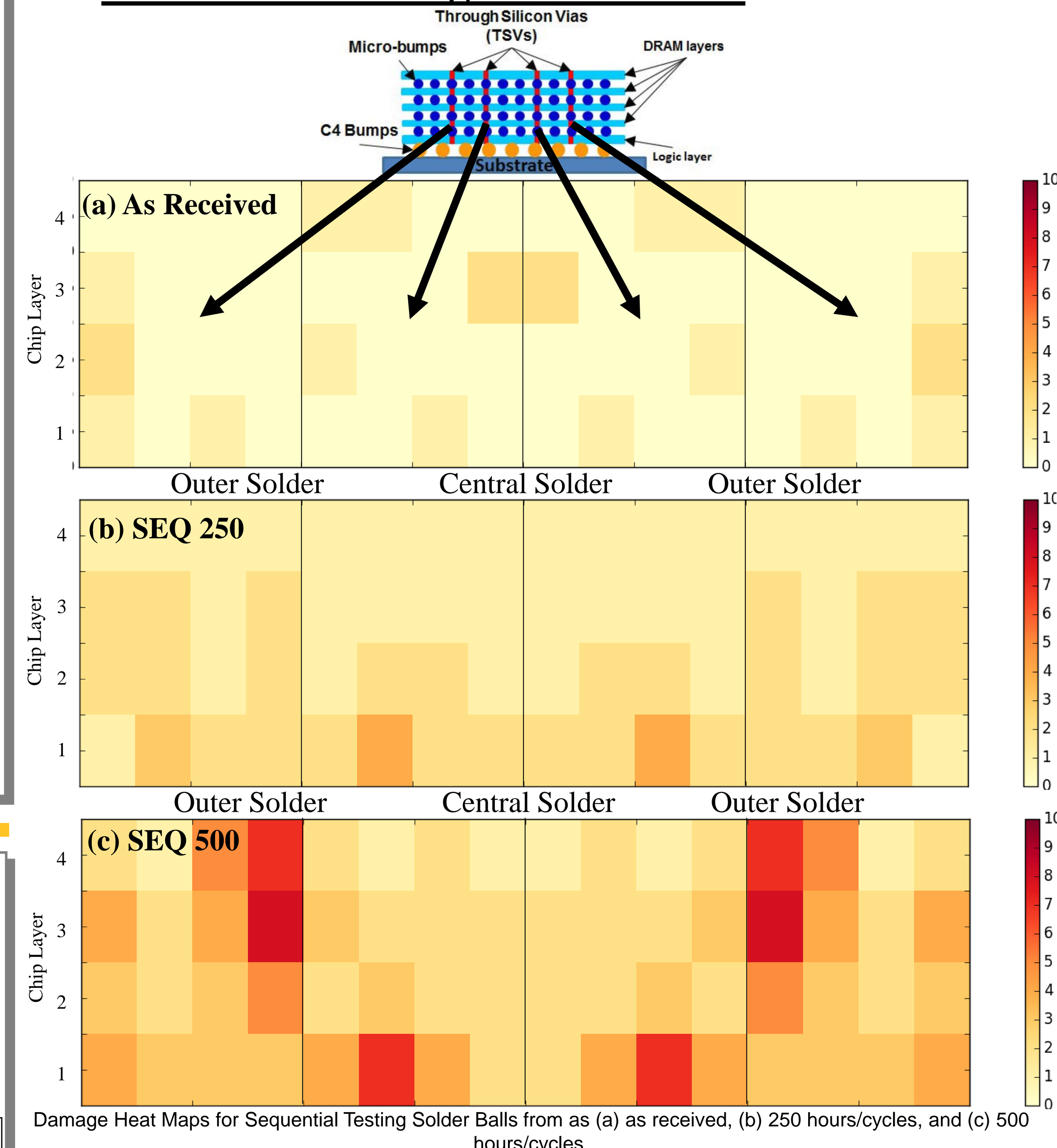
Solder Ball Composition

Via EDS scans, the solder ball composition can be confirmed, defining the regions from top to bottom as Cu, Ni, Ni_xSn_y IMCs, tin, Ni_xSn_y IMCs, Ni, and Cu. More precise scans are necessary to determine the specific MC compositions.



EDS scan on a solder ball sequentially tested for 250 hours/cycles. Solder ball is located on the 3rd layer from the bottom on the outer set of TSVs.

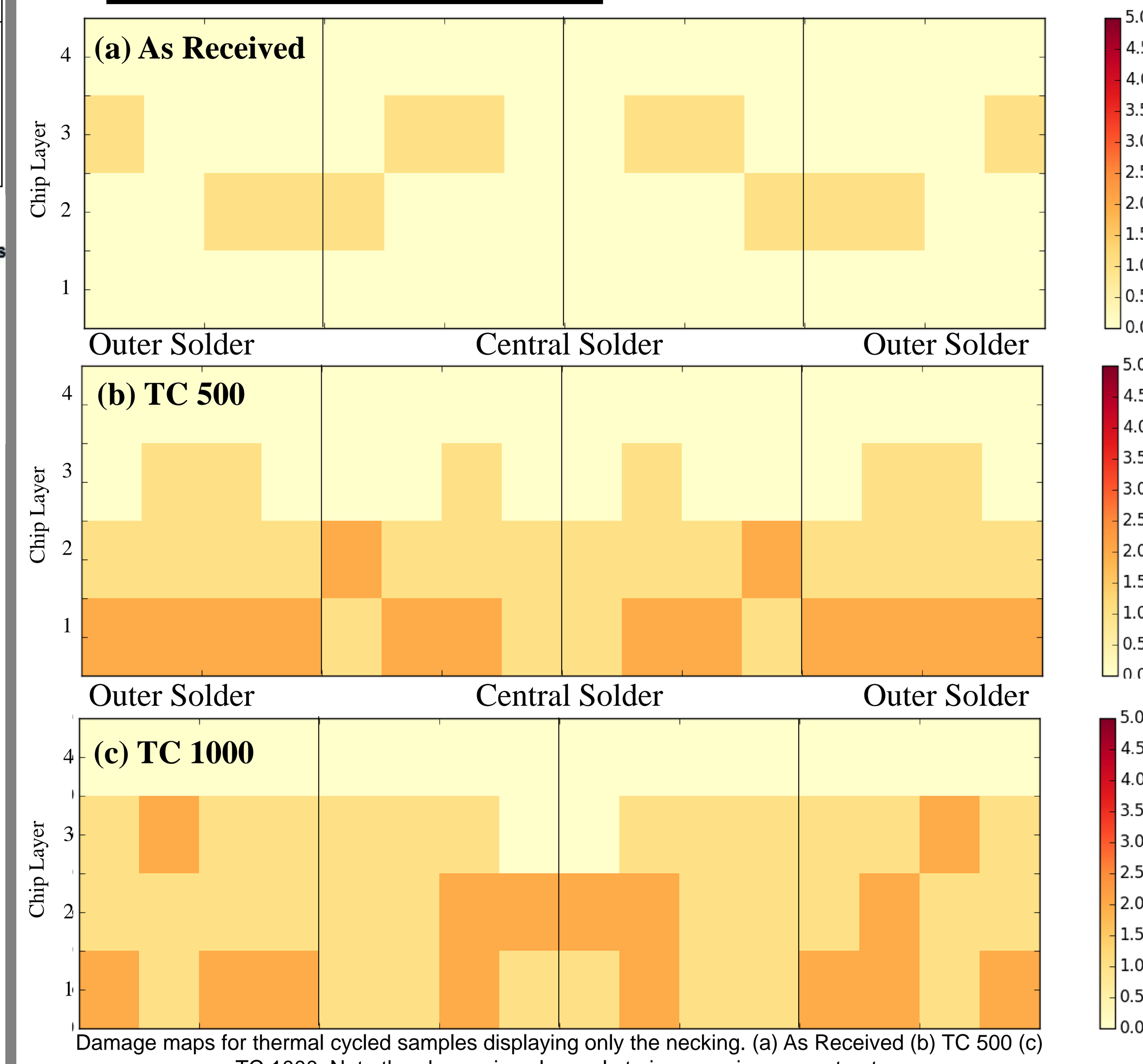
Mechanical Damage of the Solder



Damage Heat Maps for Sequential Testing Solder Balls from as (a) as received, (b) 250 hours/cycles, and (c) 500 hours/cycles.

By analyzing the mechanical damage in the solder due to cracking and necking, the damage can be mapped to the location of the solder ball. The lowest layers and near the perimeter appear more susceptible to mechanical damage over extended use. This is due to additional tin reflows and increased displacement during thermal cycling.

Solder Necking Damage

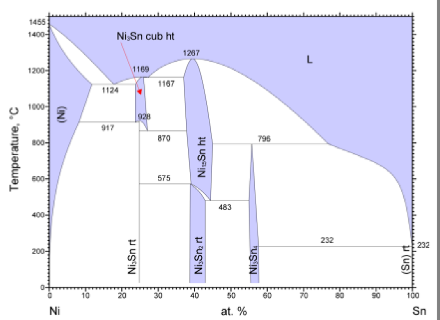


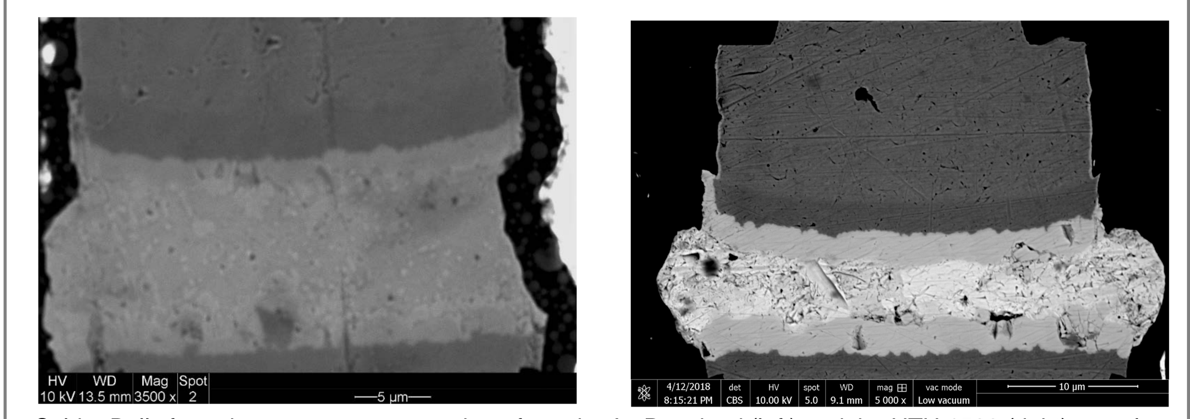
Damage maps for thermal cycled samples displaying only the necking. (a) As Received (b) TC 500 (c) TC 1000. Note the change in color scale to increase image contrast.

Analysis of the necking of the solder ball shows two distinct trends. The necking seems to increase in lower layers, however, there is very little difference from inner to outer locations. Additionally, only the early cycles appear to influence necking.

Intermetallic Growth of Ni-Sn System

The nickel layers are used as a barrier between the tin and copper. Nickel forms an IMC with tin significantly slower than with copper, helping to prevent critical failure early in the lifetime of the solder.





Solder Balls from the top row, outer quadrant from the As Received (left) and the HTH 1500 (right) samples.

$$3.28 * \frac{2T_{Ni}}{T_{Sn}} \geq 1$$

The coefficient of the inequality stems from the molar mass and density of the Ni and Sn systems

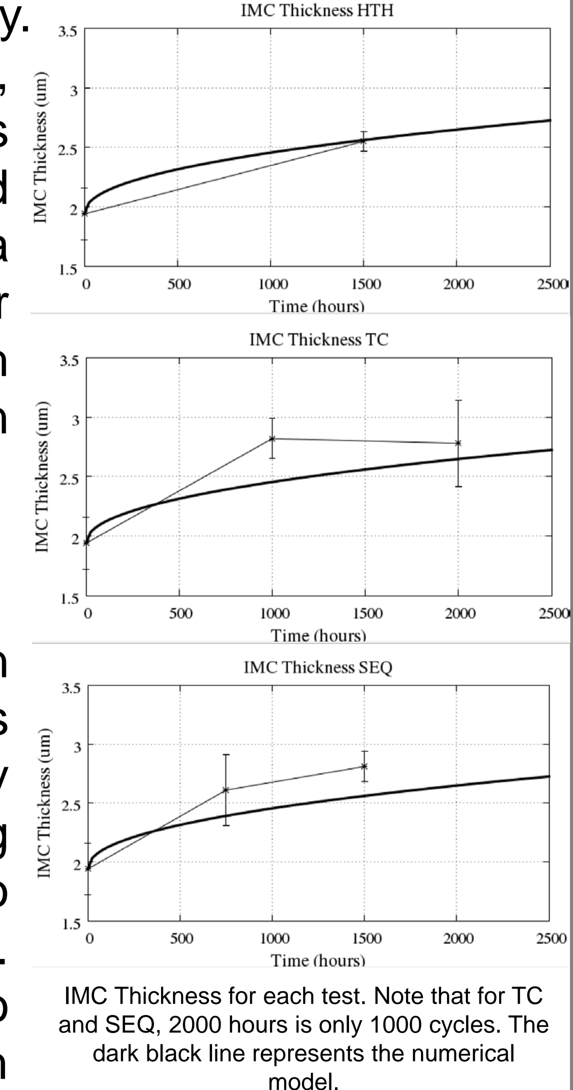
The inequality represents the necessary ratio of thickness for nickel and tin to guarantee excess nickel is present and prevent considerably amounts of copper tin intermetallic within the lifetime of the component.

Thickness Ni	Thickness Sn	Critical Ratio	Minimum CR	Necessary CR
2.34 ± .27 µm	6.25 + 1.10 µm	1.84	1.38	0.75

The nickel present is more than double the necessary size to consume the tin. The ratio minimizing boundaries values from the uncertainty still produce a significantly large ratio. Hence, the IMC regions analyzed in this study should be from the Ni-Sn system, exclusively. Through the thermal tests, the IMC growth was measured an various read points and plotted against a numerical model for constant temperature growth at 150°C fit from an Arrhenius relationship.

$$X = X_o + At^n e^{\frac{-E_a}{RT}}$$

The Ni-Sn system is known to have n value of 0.46 as well as an activation energy of -47.1 kJ/mol. The fitting constant of A was found to have a value of ~19,000. The HTH was expected to have the highest IMC growth rate, followed by SEQ, due to the largest time spent at high temperature. The difference in expected and actual trends shown can possibly be attributed to the large uncertainty in X_o value from the as received samples.



IMC Thickness for each test. Note that for TC and SEQ, 2000 hours is only 1000 cycles. The dark black line represents the numerical model.

Summary & Recommendations

Through damage analysis, it is shown that damage is more likely on solder balls near the edges of the chips and at the lower layers. This is most likely due to both increased displacement fields and multiple reflows of the solder during fabrication. It is recommended that use conditions similar to the sequential testing be avoided to prevent severe damage to the solder.